S-parameter analysis of dual gain mode fully Differential CMOS Low Noise Amplifier for Ultra Wide Band system

Md. Tanvir Ahad, Md. Mosfiqur Rahaman, Akib Yusuf, Md. Rifat Rahamatullah, Safayat-Al Imam

Abstract— The object of this paper is to observe the S-parameters of Ultra Wide band(UWB) low noise amplifier by utilizing inductively degenerated LNA with resistive feedback into the differential topology. The proposed LNA is implemented in 0.18µm RF CMOS technology considering BSIM3 model and simulated by using HSPICE. By scrupulous optimization this proposed LNA is obtained at flat gain 5.5dB, bandwidth of 5Ghz which having a low level noise figure of an amplifier. This design has a measured power gain of 14.7dB, return loss(output) of -15db at 8.4 GHz and noise figure is lower than 3db, while consuming 27 mW of D.C dissipation at 1.8 v supply voltage. This specifications adopts the ultra wide band characterizations and noise margin.

Index Terms—LNA,S-parameters, UWB, Noise figure, Noise Margin ,Bandwidth,HSPICE.

1 INTRODUCTION

Ultra-wide band (UWB) technology is considered as transmitting large amounts of digital data (about 450 Mbps) over a wide spectrum of frequency bands(3.1-10.6 GHz) with very low power for a short distance. UWB technology can enable a wide variety of applications in wireless communications, networking, radar imaging, and localizing systems. To fulfil the requirements of 802.15.3a specifications of maximum total power consumptions, a power saving concept is vital for designing an UWB transrecever. The design of low noise amplifier is the most challenging tasks in RF receivers which needs to provide low noise figure and reduce the gain of noise figure and broads the input matching and amplification of extremely low signal without adding noise and reasonable efficiency for low power consumption. Different kinds of topology are implemented for UWB LNA. Also there are different types of LNA topologies. The two well-known topology structure found are Common Source (CS) topology and Common Gate (CG) topology. There are various other possible topologies are; cascade topology, Differential topology [1].

In this paper the proposed LNA architecture used for better i/p matching where two simple inductively degenerated LNA with resistive shunt feedback is paired to make a differential LNA to get higher linearity, better input matching, higher power gain and fewer noise figure for wide band application.

- *Md. Tanvir Ahad has completed B.Sc in EEE from Ahsanullah University of Science & Technology, Dhaka, Bangladesh Email: ahadtanvir@gmail.com*
- *Md. Mosfiqur Rahaman has completed B.Sc in EEE from Ahsanullah University of Science & Technology, Dhaka, Bangladesh Email:sshaon95@yahoo.com*
- *Akib Yusuf has completed B.Sc in EEE from Ahsanullah University of Science & Technology, Dhaka, Bangladesh Email: akib147@yahoo.com*
- *Md. Rifat Rahamatullah has completed B.Sc in EEE from Ahsanullah University of Science & Technology, Dhaka, Bangladesh Email:rrahamatullah@gmail.com*
- *Safayat-Al Imam Assistant Professor, Dept. of EEE, Ahsanullah University of Science & Technology, Dhaka, Bangladesh Email:imam.safayat@gmail.com*

2 LNA CONCEPT

Low Noise Amplifier (LNA) is an electronic amplifier, located close to the detection device which can reduce the losses in the feed line. To design a perfect UWB LNA over a specified range it must have a high gain with good gain flatness. Also low noise figure, and the return loss in the feed line should also be minimized. Finally a good linearity over a range of 2Ghz is also important. Fig 1 shows the block diagram of a LNA in a system block. It is the first gain stage after antenna in the receive path, so the LNA noise figure is critical since it directly

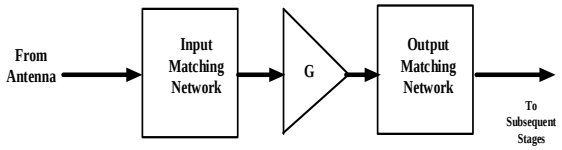

Fig 1: Block Diagram of LNA

The inductive source degeneration(IDS) method is most effective method for the architecture of LNA. It helps to increases the voltage gain of the LNA & also the output impedance. Also improve voltage gain at high frequency by cascading more devices. So with the advantage of high gain, low noise, high linearity over a wide frequency range IDS is an effective method for integrating one part of a complete low-voltage transceiver. The shunt series feedback concept can also be used for the design of an effective LNA. It helps to match input and output impedances of the system. The bias point of the input is fixed with the output voltage. Hence it can increase the power dissipation compared to other different topology with similar noise performance.

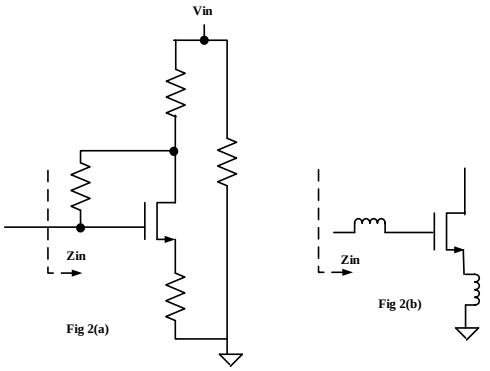

Fig 2: Common LNA architectures: (a) Shunt-series feedback (b) Inductive degeneration

For this UWB LNA paper, an inductively degenerated LNA with resistive shunt feedback is adopted with active balun circuit.

2.1 Proposed Architecture of LNA :

Fig 3 shows the simplified block diagram of the proposed LNA architecture, where two where two simple inductively degenerated LNA with resistive shunt feedback is paired to make a Differential LNA. High gain is good for LNA. as it suppress the noise effect to the subsequent stage in a system. However, usually high gain results in high nonlinearity which is not desirable. Active balun circuit helps to convert unbalanced impedance to balanced one and hence more voltage gain is possible which leads to more strong circuit against noise factor before down-converting to IF frequency. Also the active balun gives two type signals which has180^0 phase difference each other without a passive transformer [2].The proposed design uses the balun circuit for creating differential input and achieve differential output.

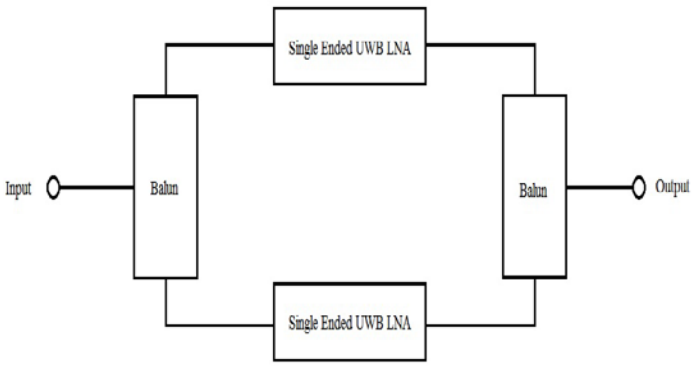

Fig 3: Simplified block diagram for proposed LNA.

2.2 Single Ended LNA

Fig 4(a) shows the circuit diagram for a UWB single ended LNA. Here cascode transistors help to avoid the amplification of the effect of capacitance between the input and output terminals known as miller effect and therefore improves the gain. Two inductors (L_s and L_g) helps for impedance matching between source resistance(R_s) and input of the LNA. The variable gain feature is realized by including an additional n-type MOSFET (M_{s1}). It helps to bypass the signal in lower gain mode. In fig 3(b) Small-signal equivalent circuit of the input of LNA is drawn . The cutoff frequency of M1 transistor (ω_t) is propotional to the Q-factor of RLC resonance circuit. Hence with the help of shunt feedback resistor(R_f) the bandwidth can be widened as well as gain can be varied within a wide range of frequencies. The q-factor can be determined by the following equation:[2].

$$Q_{wb} \approx \frac{1}{\left[R_l + \omega_t L_t + \frac{(\omega_0 L_t)^2}{R_{fM}}\right].\omega_0\left(C_{gs} + C_{d,Ms1}\right)} \quad (1)$$

here, $|R_{fm} = \frac{1}{[1-A_v]}$ and A_v is the open loop voltage gain of LNA.

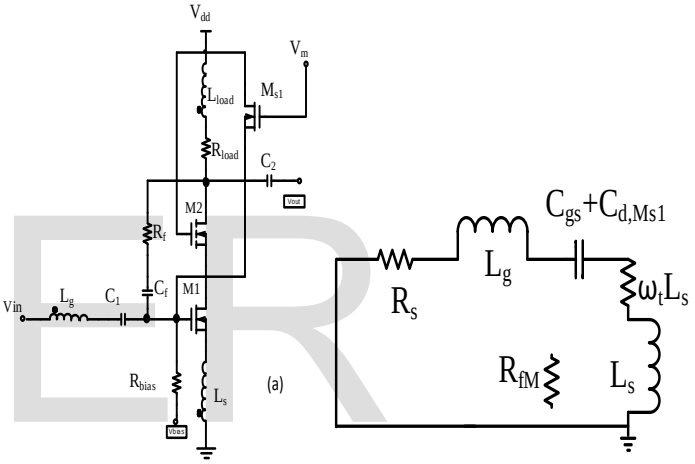

Fig 4: (a)LNA topology for UWB single ended LNA.(b) Small-signal equivalent circuit of the input of LNA [2].

3. DIFFERENTIAL LNA:

With higher immunity to environmental noise, ample amount of the noise and less interfering signals makes differential LNA adventurous over single one. The proposed differential LNA with different specifications works with different gain mode. Fig 5 shows the full-differential LNA is designed based on the single-ended LNA in previous section.

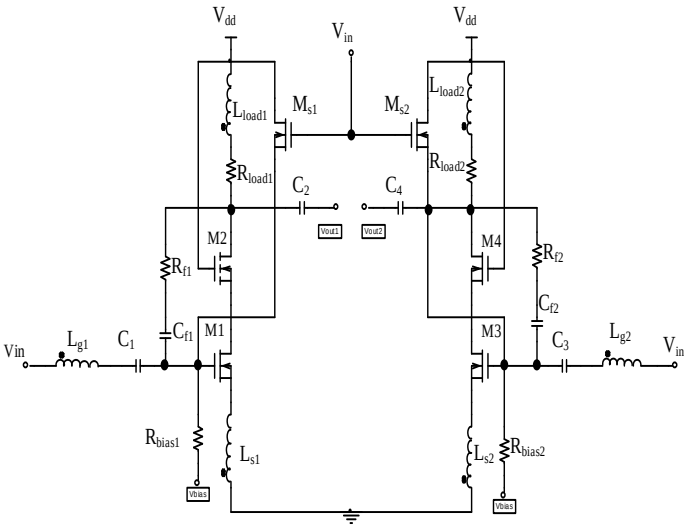

Fig 5: Differential LNA

3.1 Design Procedure:

LNA in the paper is similar specification as in ref [2]. However the analyzing parameters are different. The following table specifies the parameters:

Table 1.

Parameters	Value
Load Inductor(L_{load})	2.664nH
Output resonant frequency	≈4GHz
Source degeneration inductor (L_s)	0.17nH
The gate inductance(L_g)	2.223nH
Source Capacitance(C_{gs})	≈300fF
Feedback resistance(R_f)	1.14kΩ
Feedback capacitance(C_f)	2pF
Bias resistance (R_{bias})	1.417kΩ

2.3 Simulation results:

The design was simulated with BSIM3 model provided for 0.18µm RF CMOS process. Some of the important parameters for LNA such as input reflection coefficient with the output matched for forward transmission gain or loss(S_{21}),reverse transmission or isolation(S_{12}), output reflection coefficient with the input matched(S_{22}), power gain and noise figure are simulated in HSpice. Figures 6 to 15 show the corner simulations for each of these parameters.

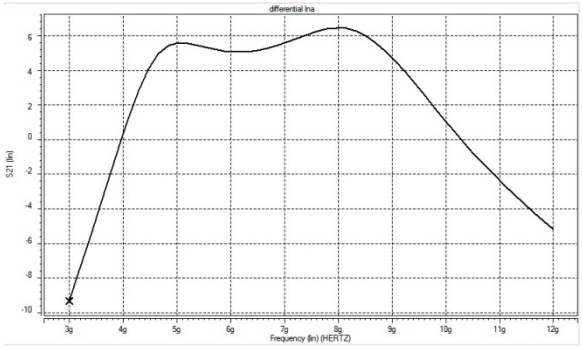

Fig 6: S_{21} (dB) of Differential LNA

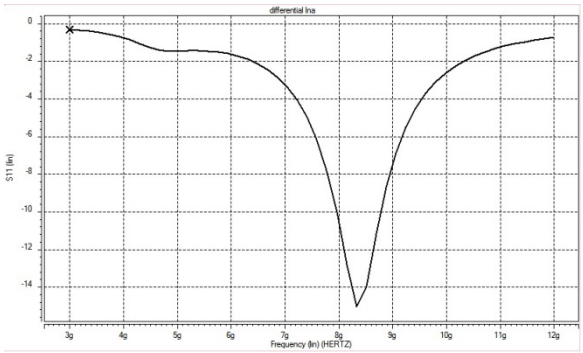

Fig 7: S_{11} (dB) of Differential LNA

Gain and input matching parameters (S_{21} and S_{11}) are plotted in Fig 4.1 to Fig 4.3 S_{21} of the proposed LNA is plotted in Fig 4.1. S_{21} is around 5.5 dB from 5 GHz to 8.7 GHz. Fig 4.2 shows S_{11} of the Differential LNA, which has a value of -15 dB at 8.4GHz. So, S_{21} and S_{11} of Fig 4.3 assure good input matching of the network.

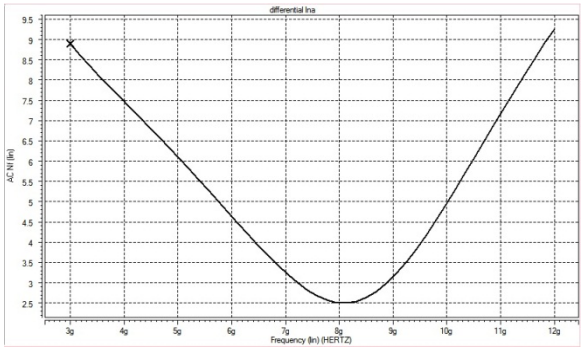

Fig 8: AC output Noise figure of Differential LNA

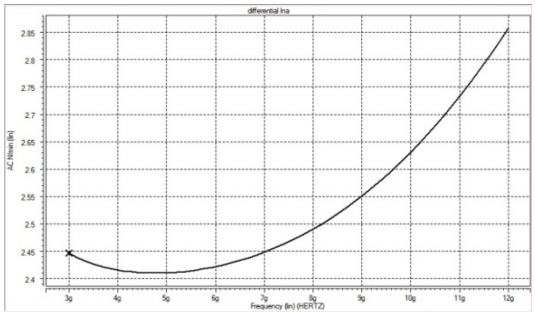

Fig 9: Minimum AC output noise figure of Differential LNA

Fig 8 shows the AC output noise figure and Fig 9 shows the stability factor of the proposed LNA. AC output noise figure is 2.5dB.

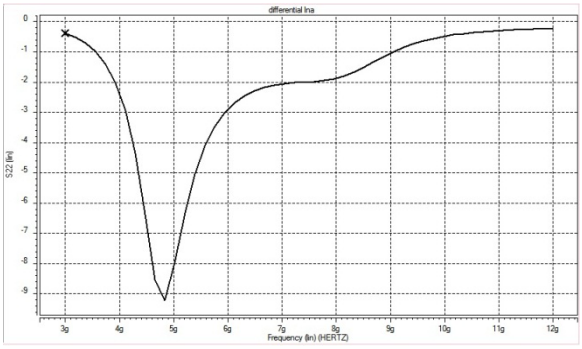

Fig 10: S_{22} of Differential LNA

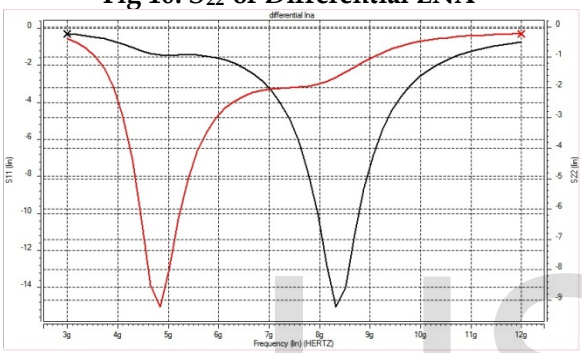

Fig 11: Comparison between S_{11} and S_{22} of Differential LAN

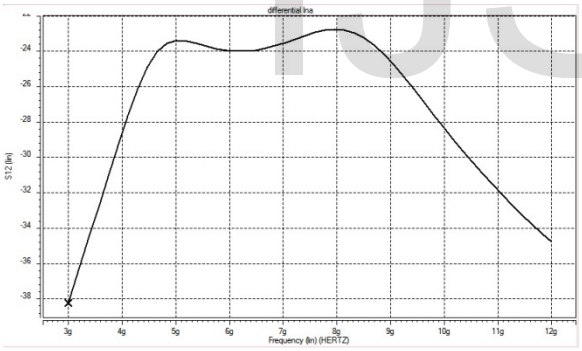

Fig 12: S_{12} of Differential LNA

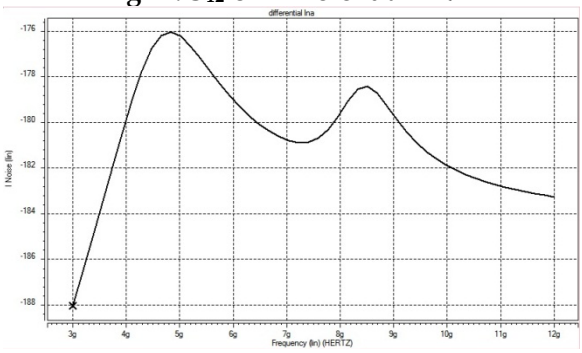

Fig 13: Output Noise of Differential LNA

Fig 12 shows the S_{12} of the LNA of this work. The output noise is shown in Fig 13.

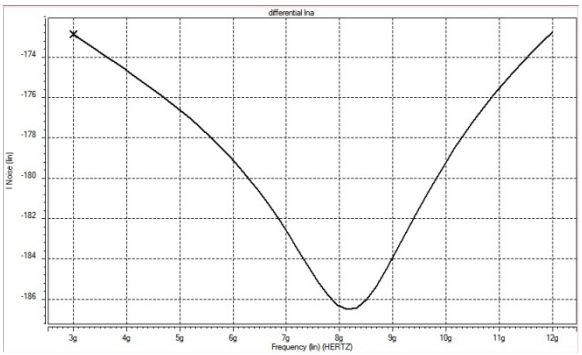

Fig 14: : Input Noise (dB) of Differential LNA

The input Noise is shown in Fig 4.10..

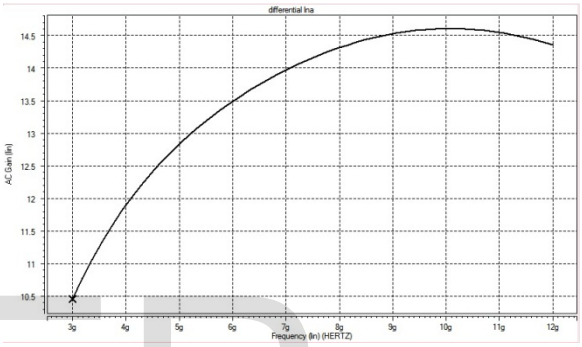

Fig 15: Maximum Power Gain of Differential LNA

Maximum power gain of the proposed LNA is shown in Fig 4.12. At 10 GHz we get the maximum power gain with a value of 14.7 dB. At center Frequency 8.4 GHz and Power Gain is more than 14dB.

Comparison of performance between Single ended LNA and Differential LNA in this paper is given in table below.

Table 2:

The performance of the proposed Differential LNA is summarized in the table below:

Parameters	Value
Frequency	8.4GHz
Power Supply Voltage	1.8v
Power Consumption	27mW
S_{21}	5.5 dB
S_{11}	-15dB
Noise Figure	2.5dB
BW_{-3dB}	7.5-10.1 GHz

Comparison with other works in the reference is given in the table below

.

Table 3:

Comparison with other LNA from the bibliography.

Ref	Tech-nology	Band width	Gain	NF	Dif-ferential	Input Match	Power
[3]	0.25µm	2-1600MHz	13.7 dB	2.5dB	no	yes	35nW
[4]	0.18µm	8-1 GHz	26dB	4.1dB	yes	yes	36mW
[5]	0.13µm	100-930 GHz	13dB	4dB	yes	yes	0.72mW
This work	0.18µm	8.5-9.4GHz	14.7 dB	2.5dB	yes	yes	27mW

3 CONCLUSION:

the proposed design improves the gain, bandwidth and noise margin by using inductively degenerated LNA. To match the input-output impedance a shunt series feedback circuit has been opted in the design. Also all the important parameters such as input and output reflection coefficient with output matched are observed for this designed LNA. This LNA can be operate successfully of different type of UMB band groups by placing different type of inductances and capacitances or different matching circuitry for each band in parallel. Corresponding the circuit application and enhancing the integrating CMOS differential LNA is designed, and it can be utilize in wireless RF receiver.

REFERENCES

[1] Gyamlani, Sunny, et al. "Comparative Study of various LNA topologies Used for CMOS LNA Design." Int. J Comp Sci. Emerging Tech 3.1 (2012): 41-49.

[2] Garuda, Chetty, et al. "A 3-5 GHz fully differential CMOS LNA with dual-gain mode for wireless UWB applications." Circuits and Systems, 2005. 48th Midwest Symposium on. IEEE, 2005.

[3] Bruccoleri, Federico, Erik AM Klumperink, and Bram Nauta. "Generating all two-MOS-transistor amplifiers leads to new wide-band LNAs." Solid-State Circuits, IEEE Journal of 36.7 (2001): 1032-1040.

[4] Adiseno, I., Hakan Magnusson, and Hakan Olsson. "A 1.8-V wideband CMOS LNA for multiband multistandard front-end receiver." Solid-State Circuits Conference, 2003. ESSCIRC'03. Proceedings of the 29th European. IEEE, 2003.

[5] Stanley B. T. Wang, Ali M. Niknejad, and Robert W. Brodersen, "A Sub-mW 960-MHz Ultra-Wideband CMOS LNA", Berkeley Wireless Research Center, Dept. of EECS, UC Berkeley, Berkeley, CA 94704, USA